

**Office Action Summary**

Application No.

09/895,151

Applicant(s)

TOKUNAGA, YUICHI

Examiner

Eric Chang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2.4.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. Claims 1-13 are pending.

#### ***Drawings***

2. The drawings are objected to because of unclear copies; the drawings contain ghost images of portions of figures. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because the label "Activation Control Means" for element 8 in FIGS. 1, 3, 4 and 6 is misspelled. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

#### ***Specification***

4. The disclosure is objected to because of the following informalities: "register 71" from the drawings is inconsistently referred to as "resister 71" throughout the specification; an example may be found on line 14 of page 11.

Appropriate correction is required.

5. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. **For example,**

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please change the term “poser” on line 20 of page 6 to “power”; and the transitive verb “inactivate” on line 9 of page 7 is used as an adjective.

### ***Claim Objections***

6. Claim 2 is objected to because of the following informalities: the phrase “as to at” in line 3 of the claim is unclear. Appropriate correction is required.

7. Claim 9 is objected to because of the following informalities: the term “poser” in line 2 of the claim should read, “power”. Appropriate correction is required.

8. Claim 13 is objected to because of the following informalities: the transitive verb “inactivate” on line 3 of the claim is used as an adjective. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an

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international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

10. Claims 1-2, 8-11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,240,521 to Barber et al.

11. As to claim 1, Barber discloses a multiprocessor apparatus (10) comprising: a high speed processor (42) operating at a high speed [col. 1, lines 65-67, and col. 2, lines 1-2]; a low speed processor (44) operating at a low speed [col. 1, lines 65-67, and col. 2, lines 1-2]; and an activation controller (40) for controlling activation and inactivation of each of said high speed processor and said low speed processor based on application program to be processed [col. 2, lines 13-20, and col. 5, lines 2-10]. Barber teaches a multiprocessor apparatus that uses a high speed processor for executing computationally intensive software, and a low speed processor for executing less demanding software, substantially as claimed.

12. As to claim 2, Barber discloses determining which of said processors application program is to be processed, wherein said activation controller controls activation and inactivation of each of said high speed processor and said low speed processor based on a determination result [FIG. 8, elements 132 and 140, and col. 6, lines 8-39].

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13. As to claim 8, Barber discloses said activation controller places the respective processors into a sleep state or an active state, which inherently comprises activating and stopping clock signals for said processors [col. 3, lines 5-15] , substantially as claimed.

14. As to claim 9, Barber discloses said activation controller places the respective processors into a sleep state or an active state, which inherently comprises activating and stopping power sources for said processors [col. 3, lines 5-15] , substantially as claimed.

15. As to claim 10, Barber discloses said low speed processor has minimum function required for processing said application program at a low speed [col. 5, lines 49-59].

16. As to claim 11, Barber discloses said low speed processor uses a low voltage and a low frequency clock [col. 5, lines 49-59].

17. As to claim 13, Barber discloses said low speed processor requires said activation controller to deactivate said low speed processor after completion of processing of said application program [col. 3, lines 65-67, and col.4, lines 1-35]. Barber teaches that each of the processors is deactivated after its respective execution of a program. Therefore, Barber teaches that the low speed processor is deactivated after completion of its application program, substantially as claimed.

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18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,240,521 to Barber et al., in view of U.S. Patent 6,035,408 to Huang.

20. As to claim 3, Barber discloses a multiprocessor apparatus comprising: a high speed processor operating at a high speed [col. 1, lines 65-67, and col. 2, lines 1-2]; a low speed processor operating at a low speed [col. 1, lines 65-67, and col. 2, lines 1-2]; and an activation controller for controlling activation and inactivation of each of said high speed processor and said low speed processor based on application program to be processed [col. 2, lines 13-20, and col. 5, lines 2-10]. Barber teaches all of the limitations of the claim, including that each processor is selectively activated by an activation controller, but does not teach the activation controller comprises a switch for selectively coupling a high-speed processor and a low-speed processor via their respective busses to a memory.

Huang teaches a bus coupling unit which couples a high speed bus for coupling said high speed processor and a low speed bus for coupling said low speed processor, wherein said bus coupling unit includes a switch coupled to a memory, for switching connection and disconnection between said memory and said high speed bus [col. 1, lines 66-67, and col. 2, lines

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1-15]. Huang teaches that each processor is connected to its respective bus [FIG. 2], and that a switch is used to selectively coupling each processor to a memory.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the switch means as taught by Huang. One of ordinary skill in the art would have been motivated to do so that each processor may be selected for operation by coupling it to the system memory.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of selecting either a high-speed processor or a low-speed processor to activate and execute software within a computer system. Moreover, the switch means taught by Huang would improve the flexibility of Barber because it allowed for the detection of the power source of the computer system to also inform the choice of processor, in addition to the software requirements, as taught by Barber.

21. As to claim 12, Barber discloses a processor selection latch (90), wherein the contents of said latch is changed based on a result of determination of said processing determining unit, and said activation controller controls an activation state of said processor based on the contents of said latch [col. 5, lines 2-10]. Barber teaches that the latch is set to indicate the desired processor, and that the latch controls the operation of the selected processor. It would have been obvious to one of ordinary skill that the latch may also be implemented as any other type of value-containing memory device, such as a register, substantially as claimed.

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22. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,240,521 to Barber et al., in view of U.S. Patent 5,584,010 to Kawai et al.

23. As to claim 4, Barber discloses a multiprocessor apparatus comprising: a high speed processor operating at a high speed [col. 1, lines 65-67, and col. 2, lines 1-2]; a low speed processor operating at a low speed [col. 1, lines 65-67, and col. 2, lines 1-2]; and an activation controller for controlling activation and inactivation of each of said high speed processor and said low speed processor based on application program to be processed [col. 2, lines 13-20, and col. 5, lines 2-10]. Barber teaches all of the limitations of the claim but does not teach that each processor is coupled to its own memory.

Kawai teaches that each processor is coupled to a respective memory via a respective bus, wherein the memory stores data and program required for said processor to process an application program [FIGS. 5 and 6, and col. 17, lines 50-55].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the individual buses and memories for each processor as taught by Kawai. One of ordinary skill in the art would have been motivated to do so that data and program for each processor may be transferred to the other processor.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of transferring data between multiple processors in a computer system. Moreover, the configuration means taught by Kawai would improve the flexibility of Barber because it allowed for more than two processors to transfer data within a computer system.

24. As to claim 5, Barber discloses a memory which stores data and program necessary for transferring said data and program required for said low speed processor to process said application program from said memory coupled to said high speed bus to said memory coupled to said low speed bus [FIG. 6, element 86, and col. 5, lines 2-10]. Barber teaches a static memory for saving the machine state of the computer system in order to facilitate the transfer of the execution between the low-speed processor and the high-speed processor, substantially as claimed.

25. As to claim 6, Kawai discloses a DMA circuit for transferring said data and program required for said low speed processor to process said application program from said memory coupled to said high speed bus to said memory coupled to said low speed bus [col. 17, lines 56-59].

26. As to claim 7, Kawai discloses said low speed processor transfers said data and program required for said low speed processor to process said application program from said memory coupled to said high speed bus [col. 4, lines 61-65]. Kawai teaches transferring data and program from one processor to the memory coupled to another processor, substantially as claimed.

### ***Conclusion***

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27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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April 21, 2004